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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/674,886
Filing Date: September 30, 2003
Appellant(s): KIM ET AL.

Patrick J. Buckley (40,928)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 07 November 2006 appealing from the Office action mailed 11 January 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct. Although Applicant has added extra information for the sake of clarity, Applicant does state each of the limitations of the sole independent claim, claim 1. Specifically, regarding claim 1, Applicant states an apparatus comprising: a first voltage plane having a first conducting portion to be at a first voltage (pg. 2 of the Brief, final paragraph, lines 1-4) a signal layer on one side of the first voltage plane (pg. 2 of the Brief, final paragraph, lines 4-5); a second voltage plane on the other side of the first voltage plane

and having a second conducting portion to be at a second voltage (pg. 2 of the Brief, final paragraph, line 5 – pg 3, same paragraph, line 7); and a plurality of floating microstrip line traces on the signal layer, wherein each microstrip line is, (i) electrically connected to the second conducting portion at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion at the second end (pg. 3 of the Brief, same paragraph, lines 7-11). No dependent claim is argued separately.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US 6,172,305 B1 granted to Tanahashi, Shigeo published 9 January 2001.

US 6,188,296 B1 granted to Nibe et al. published 13 February 2001.

US 6,288,900 B1 granted to Johnson et al. published 11 September 2001.

US 6,243,261 B1 granted to Janik et al. published 5 June 2001.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3, 5, 7-10, 12-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,172,305 (Tanahashi)

Tanahashi discloses, referring to figures 3a-c, an apparatus, comprising: a first voltage plane (12) having a first conducting portion (P2) to be at a first voltage; a signal layer (14, comprising S2) on one side of the first voltage plane; a second voltage plane (11) on the other side of the first voltage plane and having a second conducting portion (G1) to be at a second voltage; and a plurality of floating microstrip line traces (G4 one shown, a plurality referred to, see col. 16, lines 55-60) on the signal layer. While Tanahashi does specifically show one microstrip line electrically connected to the second conducting portion at a first end (via T2) not directly connect to any other microstrip line at a second end opposite the first end and not directly connect to the second conducting portion at the second end, Tanahashi does not specifically state that each microstrip line is connected to said second conducting portion [claims 1, 14, 18]. However, it would have been obvious to one having ordinary skill in the art at the time of invention to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow.

Additionally, the modified invention of Tanahashi teaches wherein the first voltage plane is a power plane (P2) and the second voltage plane is a ground plane (G1) [claim 2], wherein the microstrip line and the second voltage plane are electrically connected via a plated through hole (T2) [claim 5], wherein the microstrip line provides impedance damping (see col. 2, lines 60-65) [claim 7], wherein the microstrip line reduces resonance between the first voltage plane and the second voltage plane (see col. 2, line 60 – col. 3, line 5) [claims 8, 19], wherein the first voltage plane, the signal layer, and the second voltage plane are separated by a dielectric material (14, 13) [claim 9], wherein the apparatus is a printed circuit board and the microstrip lines are positioned substantially around the perimeter of the board [claim 10], further comprising: a second signal layer (S1) [claim 12] and positioning the microstrip line in the signal layer to reduces cross-talk (see col. 6, lines 20-35) [claim 15]

Moreover, although the modified invention of Tanahashi does not specifically state a plurality of second microstrip lines each microstrip line is electrically connected to the second voltage plane at a first end (see col. 17, lines 45-60) not directly connect to any other microstrip line at a second end opposite the first end and not directly connect to the second voltage plane at the second end [claims 13, 16], such a modification would only involve creating a signal layer substantially identical to the signal layer previously described. Since Tanahashi clearly teaches adding additional layers similar to the explicitly described layers to the invention (col. 16, lines 50-60), it would have been obvious to one having ordinary skill in the art at the time of invention

to add such a signal layer. The motivation for doing so would have been to allow for more signal routing. Additionally, it would have been obvious to one having ordinary skill in the art at the time of invention to connect the microstrip lines to the same voltage plane. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow.

Similarly, regarding claims 1 & 3, Tanahashi discloses, referring to figures 3a-c, an apparatus, comprising: a first voltage plane (12) having a first conducting portion (G2) to be at a first voltage; a signal layer (14, comprising S2) on one side of the first voltage plane; a second voltage plane (11) on the other side of the first voltage plane and having a second conducting portion (P1) to be at a second voltage; and a plurality of floating microstrip line traces (P4 one shown, a plurality referred to, see col. 16, lines 55-60) on the signal layer. While Tanahashi does specifically show one microstrip line electrically connected to the second conducting portion at a first end (via T5) not directly connect to any other microstrip line at a second end opposite the first end and not directly connect to the second conducting portion at the second end, Tanahashi does not specifically state that each microstrip line is connected to said second conducting portion [claims 1, 14]. However, it would have been obvious to one having ordinary skill in the art at the time of invention to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow. Also, Tanahashi

teaches wherein the first voltage plane is a ground plane (G2) and the second voltage plane is a power plane (P1) [claim 3].

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanahashi as applied to claim 1 above, and further in view of US 6,188,296 (Nibe).

Tanahashi teaches the claimed invention as described above except Tanahashi does not specifically state that each microstrip line is substantially 15μm thick. However, it is well known in the art to form microstrip lines with this thickness as evidenced by Nibe (see col. 7, lines 20-25). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form each microstrip line in the invention of Tanahashi to be 15μm thick as is known in the art and evidenced by Nibe. The motivation for doing so would have been to tailor the characteristic impedance to a desired value. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanahashi as applied to claim 10 above, and further in view of US 6,288,900 (Johnson).

Tanahashi discloses the claimed invention as described above except Tanahashi does not specifically state the printed circuit board is associated with at least one of: (i) a flip chip ball grid array package model, and (ii) a pin grid array package model (col. 4, lines 5-20) [claim 11]. Instead Tanahashi generically states that the board is to be

associated with "a semiconductor integrated circuit device". Flip chip ball grid arrays (FC/BGA) are well known semiconductor integrated circuit devices as evidenced by Johnson (see col. 1, lines 1-5). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to replace the generic "semiconductor integrated circuit device" of the invention of Tanahashi with a FC/BGA as is well known in the art and evidenced by Johnson. The motivation for doing so would have been to use a package with a small footprint thus not needlessly squandering board space.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,243,261 (hereafter Janik) in view of Tanahashi.

Janik discloses a PCB coupled to a DRAM [claim 20] and a processor [claim 21]. Janik does not disclose the particulars of the PCB. Tanahashi teaches, referring to figures 3A-C, a first voltage plane (11) having a first conducting portion (G2) to be at a first voltage; a signal layer (14, comprising S2) on one side of the first voltage plane; a second voltage plane (11) on the other side of the first voltage plane and having a second conducting portion (G1) to be at a second voltage and a plurality of floating microstrip line traces (G4) on the signal layer. Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the PCB taught by Tanahashi in the invention of Janik. The motivation for doing so would have been to use a circuit board with enhanced protection against cross talk, resulting in a more reliable device. Janik in view of Tanahashi does not specifically state that each microstrip line is connected to said second conducting portion. However, it would have

been obvious to one having ordinary skill in the art at the time of invention to connect each of the microstrip lines to the portion (G1) in similar fashion as the expressly shown microstrip line (G4) since this fashion is taught by Tanahashi. The motivation for doing so would have been to ensure that each line is at the same voltage, thus avoiding any unwanted current flow.

(10) Response to Argument

Firstly, Applicant alleges, referring to page 3 of Applicant's Brief, "neither P2 nor layer 12 is a voltage plane". Although Applicant admits that layer 12 does contain a conductive portion set to a specific voltage (i.e. P2), Applicants seem to allege that the presence of additional conductive portion G2 on layer 12, would prevent the ordinarily skilled artisan from recognizing layer 12 as a "first voltage plane". However, the Examiner asserts that Applicant has provided no specific special definition to the term "first voltage plane" and further that in determining the broadest reasonable interpretation of the term "first voltage plane" consistent with the specification, the ordinarily skilled artisan would define "first voltage plane" as simply a first plane, which provides a voltage. Indeed, it is clear that the layer 12, as disclosed in figures 3A – 3C of Tanahashi is, in fact a planar object, which provides a voltage via the conductive portion P2 (see also col. 14, lines 40-50). Thus, it is the Examiner's position that the instantly claimed "first voltage plane" is indeed taught by Tanahashi. The presence of other types of wiring (e.g. ground wiring G2) does not prevent the layer 12 from performing as a first voltage plane.

Secondly, and similarly, Applicant alleges, referring to page 3 of Applicant's Brief, "layer 11 is not a voltage plane". Although Applicant admits that layer 11 does contain a conductive portion set to a specific voltage (i.e. G1), Applicants seem to allege that the presence of additional conductive portions P1 and S1 on layer 11, would prevent the ordinarily skilled artisan from recognizing layer 11 as a "second voltage plane". However, the Examiner asserts that Applicant has provided no specific special definition to the term "second voltage plane" and further that in determining the broadest reasonable interpretation of the term "second voltage plane" consistent with the specification, the ordinarily skilled artisan would define "second voltage plane" as simply a second plane, which provides a voltage. Indeed, it is clear that the layer 11, as disclosed in figures 3A – 3C of Tanahashi is, in fact a planar object, which provides a voltage via the conductive portion G1 (see also col. 14, lines 40-50). Thus, it is the Examiner's position that the instantly claimed "second voltage plane" is indeed taught by Tanahashi. The presence of other types of wiring (e.g. power wiring P1 and signal wiring S1) does not prevent the layer 11 from performing as a second voltage plane.

Thirdly, Applicant alleges that Tanahashi does not teach the limitation "a 'plurality' of floating microstrip line traces on the signal layer". Applicant asserts that the passage from col. 16, lines 55-60 which states:

> Further, a plurality of wiring conductors may be placed for each kind, and various multilayer circuit boards configured by the first to four insulating layers I1 to I4 may be combined and overlaid on the multiplayer circuit board configured by the first to fourth insulating layers I1 to I3.

"refers to additionally layers being added to the circuit board and does not disclose or suggest that a plurality of floating microstrip lines may be provided on the signal layer as recited in the claims" (emphasis Applicant's). The Examiner agrees that the "various multilayer circuit boards configured by the first to four insulating layers I1 to I4 may be combined and overlaid on the multiplayer circuit board configured by the first to fourth insulating layers I1 to I3" portion does indeed teach additional circuit layers. However, the portion that reads, "a plurality of wiring conductors may be placed for each kind", teaches that for each kind of wiring conductor disclosed in the invention a plurality of such conductors may be provided. Thus, this passage would suggest to the ordinarily skilled artisan that though only one of any such wiring is expressly depicted in the figures, multiple such wiring is contemplated. As the Examiner has stated in the Final Rejection, Tanahashi does indeed expressly show one such floating microstrip line trace (G4) on the signal layer. And though not shown in the figures, as stated in the above quoted passage from col. 16, lines 55-60, a plurality of such floating microstrip line traces is contemplated.

Thus, having addressed each of Applicant's arguments, the Examiner asserts that the traversal of the Final Rejection on these grounds is unsuccessful and respectfully submits that the Final Rejection should be affirmed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Conferees:

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